In The Claims:

Please amend the claims in the application according to the following listing of claims.

1. (Currently amended) A chip package structure, at least comprising:

a carrier having a surface, a power pad and a ground pad, said surface having a die bonding area, said power pad and said ground pad being on said surface, said power pad and said ground pad being disposed outside said die bonding area;

a die having an active surface and a backside corresponding to said active surface, said backside being attached to said die bonding area on said surface of said carrier, said die having a plurality of die pads on said active surface;

at least a passive component disposed between said power pad and said ground pad, said passive component having at least two electrodes electrically and physically connected to said power pad and said ground pad respectively, wherein a metal layer directly formed on the electrodes and said metal layer directly formed on the electrodes includes Ni, Au, or Ni/Au alloy; and

at least a first conducting wire having two ends physically connected to one of said plurality of die pads and one of said electrodes, respectively, wherein one of said die pads is electrically connected to said power pad or said ground pad via the first conductive wire and one of said electrodes of said passive component and said metal layer directly formed on the electrodes enhances the connection property between said first conducting wire and one of said electrodes.

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2. (Original) The chip package structure of claim 1, further comprising a dielectric material covering said die, said passive component, and said first conducting wire.

3. (Original) The chip package structure of claim 1, wherein said carrier comprises a signal pad, said signal pad being disposed outside said die bonding area and farther from said die bonding area than said power pad and said ground pad.

4. (Original) The chip package structure of claim 3, further comprising at least a second conducting wire having two ends connected to another one of said plurality of die pads and said signal pad respectively, said second conducting wire crossing over said passive component.

5. (Original) The chip package structure of claim 4, further comprising a dielectric material covering said die, said passive component, said first conducting wire, and said second conducting wire.

Claim 6. (Cancelled)

7. (Original) The chip package structure of claim 1, wherein said passive component is selected from one of an inductor and a capacitor.

8. (Original) The chip package structure of claim 1, wherein said carrier is a package substrate.

9. (Currently amended) A wire bonding package structure for electrically connecting a die to a carrier, said carrier having a surface and a die bonding area on said surface, said die having an active surface and a backside corresponding to said active surface, said backside of said die being attached to die bonding area, said wire bonding package structure at least comprising:

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a power pad on said surface of said carrier;

a ground pad on said surface of said carrier;

a signal pad on said surface of said carrier, said power pad, said ground pad and said signal pad being disposed outside said die bonding area, wherein said signal pad being farther from said die bonding area than said power pad and said ground pad;

a passive component disposed between said power pad and said ground pad, said passive component having at least two electrodes electrically and physically connected to said power pad and said ground pad respectively, wherein a metal layer directly formed on the electrodes and said metal layer directly formed on the electrodes includes Ni, Au, or Ni/Au alloy;

a plurality of die pads on said active surface of said die;

a first conducting wire having two ends electrically and physically connected to one of said die pads and one of said electrodes respectively; and

a second conducting wire having two ends electrically and physically connected to another one of said die pads and said signal pad respectively, wherein said second conducting wire crossing over said passive component, wherein one of said die pads is electrically connected to said power pad or said ground pad via the first conductive wire and one of said electrodes of said passive component and said metal layer directly formed on the electrodes enhances the connection property between said first conducting wire, said second conducting wire and one of said electrodes.

Claim 10. (Cancelled)

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11. (Original) The wire bonding package structure of claim 9, wherein said passive component is selected from one of an inductor and a capacitor.

12. (Original) The wire bonding package structure of claim 9, further comprising a dielectric material covering said die, said passive component, said first conducting wire, and said second conducting wire.

13. (Original) The wire bonding package structure of claim 9, wherein said carrier is a package substrate.

Claims 14 - 19. (Cancelled)

20. (new) A chip package structure, at least comprising:

a carrier having a surface, wherein the surface has a die bonding area, a power pad, and a ground pad, wherein the power pad and ground pad are disposed outside the die bonding area;

a die disposed on the die bonding area of the surface of the carrier, wherein the die has a plurality of die pads;

at least one passive component having two electrodes, wherein the electrodes are connected to the power pad and the ground pad respectively;

a metal layer formed on the electrode; and

at least one first conductive wire having two ends, wherein one end is connected to one die pad of the die, and the other end contacts the metal layer of one electrode of the passive component.

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21. (new) The chip package structure of claim 20, further comprising a dielectric material covering the die, the passive component, and the first conductive wire.

22. (new) The chip package structure of claim 20, wherein the carrier has a signal pad disposed outside the die bonding area, wherein the signal pad is disposed outside the region between the power pad and ground pad.

23. (new) The chip package structure of claim 22, further comprising at least one second conductive wire having two ends, wherein one end is connected to one die pad of the die, and the other end is connected to the signal pad.

24. (new) The chip package structure of claim 20, wherein one first conductive wire crosses over one electrode of the passive component and contacts the metal layer of the other electrode of the passive component.

25. (new) The chip package structure of claim 20, wherein the carrier is a package substrate.

26. (new) The chip package structure of claim 20, wherein the metal layer includes Ni, Au, or Ni/Au alloy.

27. (new) The chip package structure of claim 20, wherein one first conductive wire does not cross over the passive component.

28. (new) The chip package structure of claim 20, wherein the passive component is an inductor or a capacitor.

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